Remarks:

Claims 1 to 30 are pending. The Declaration filed with this application has been objected to as stating U.S. Parent Application Number "10/155,512", which should be "10/155,502". The Abstract has been objected to. Claims 1-30 stand rejected under 35 USC 112 second paragraph. Claims 16-30 stand rejected under 35 USC 101. Claims 1-30 would be allowable if rewritten to overcome these rejections.

Objections to the Abstract

The Abstract stands objected as using superfluous language (i.e. "present invention includes" and containing an undefined acronym ("DSP"). The abstract should be limited to a single paragraph within the range of 50 to 250 words. The abstract has been amended to address these objections as follows:

> ~~*The invention includes a*~~ *A method and apparatus for generating a wide instruction controlling at least one data processing resource, local to that data processing resource, by accessing a local wide instruction memory based upon a narrow instruction, to generate at least part of the wide instruction. The local wide instruction memory can be accessed on every instruction cycle to reconfigure the controlled data processing resource(s). The data processing resources preferably includes arithmetic resources acting on the logarithms of various data inputs to generate a spectrum of non-additive results. A preferred embodiment permits the narrow instruction to include a designator field, a first narrow field and a second narrow field. The designator field is used by the local wide instruction memories to select which of the first and second narrow fields to use in accessing the memory for controls of a specific resource. Use in a graphics shader with four datapath columns is shown. Another preferred use is shown in a Digital Signal Processor (DSP) is also shown.*

Consequently, the Applicant requests that this objection be removed.

Objection to Declaration

The Declaration filed with this application has been objected to as stating U.S. Parent Application Number "10/155,512", which should be "10/155,502". The specification has been amended as follows:

Serial Number 10/276,41, docket number ARITH001US, filed Nov. 12, 2002, which is the national stage application based upon, Serial number PCT/US 01/15,541, entitled "Method and apparatus of DSP resource allocation and use", filed May 14, 2001 by Jennings, docket number ARITH001; ~~*and*~~

Serial number 10/226,735, entitled "Method and apparatus for high speed calculation of nonlinear functions and networks using non-linear function calculators in digital signal processing", docket number ARITH003, filed August 22, 2002; *and*

Serial number 10/155,502, filed May 23, 2002.

Consequently, the Applicant requests that this objection be removed.

Rejections under 35 USC 112 second paragraph

In Claim 1, the terms "N_logalu" and "logalu" seem mixed up. Similarly in independent claim 16. These Claims have been amended as follows:

1. (Currently amended) An apparatus operating ~~*an N_logalu*~~ *a first number of a logalu, each using a wide instruction, comprising:*

a narrow instruction provided to a local wide instruction memory;

said local wide instruction memory at least partly creating said wide instruction in response to said narrow instruction;

said logalu receiving said wide instruction;

said logalu configured based upon said wide instruction to operate upon ~~N_log_operands~~ a second number of a log-operand;

wherein said ~~N_logalu~~ first number is at least one; and

wherein said ~~N_log_operands~~ second number is at least two.

16. (currently amended) A method of operating ~~an N_logalu~~ a first number of a logalu using a wide instruction, comprising the steps of:

~~providing a narrow instruction to~~ a local wide instruction memory receiving a narrow instruction;

said local wide instruction memory responding to said narrow instruction to at least partly create said wide instruction;

said logalu receiving said wide instruction;

~~configuring~~ said logalu configured based upon said wide instruction to operate upon ~~N_log_operands~~ a second number of a log-operand;

wherein said ~~N_logalu~~ first number is at least one; and

wherein said ~~N_log_operands~~ second number is at least two.

The Applicant contends that the use of N_logalu was as a designation of a number, for convenience labeled a first number, and the use of N_log_operands was as a designation of another number, for convenience labeled a second number. These labels have been added strictly to address the rejection of the Examiner and as such do not constitute the introduction of new matter, in that the number of logalus and the number of log operands they use is a matter of observation from the initially filed application. The Applicant is the inventor as well as a registered patent agent, and acknowledges that these statements have the effect of an affidavit. Consequently the Examiner is requested the removal of this rejection from these Claims.

Based upon the amendment of Claims 1 and 16, claims 2 and 17 have been amended as follows:

2. (currently amended) The apparatus of Claim 1, wherein said ~~N_logalu~~ first

number is at least two.

17. (Original) The method of Claim 16, wherein said ~~N_logalu~~ first number is at least two.

In dependent claim 3, it is unclear whether the term "said logalu" refers to "said logalu" or "said N_logalu". This language appears redundant with the independent claim. Similarly in dependent Claim 18. These claims not been amended, in that the above amendments clarify these claims fully. Consequently the Examiner is requested the removal of this rejection from these Claims.

In dependent claim 5, the last two lines seem to be redundant language in Claim 4. Similarly in dependent claim 20. These claims have been cancelled.

In claim 6, it is unclear whether "a local wide memory" in line 6 is the same as "a local wide memory" in claim 1 line 2. Similarly in Claim 21. These Claims have been amended as follows:

6. (currently amended) The apparatus of Claim 1, wherein said narrow instruction is comprised of a designator field, a first narrow field and a second narrow field;

wherein said local wide instruction memory responding to said narrow instruction, is further comprised of:

a means for selecting from said first narrow field and said second narrow field based upon said designator field to provide a selected narrow instruction to ~~a~~ said local wide memory; and

said local wide memory responding to said selected narrow instruction to at least partly create said wide instruction.

21. (currently amended) The method of Claim 16, wherein said narrow instruction is comprised of a designator field, a first narrow field and a second

narrow field;

wherein the step said local wide instruction memory responding to said narrow instruction, is further comprised of the steps of:

a selection configuration circuit selecting from said first narrow field and said second narrow field based upon said designator field to provide a selected narrow instruction to ~~a~~ said local wide memory; and

said local wide memory responding to said selected narrow instruction to at least partly create said wide instruction.

Consequently the Examiner is requested the removal of this rejection from these Claims.

Rejections under 35 USC 101

The Examiner has rejected Claims 16-30 as reciting a method for performing a mathematical function. These Claims have been amended as follows:

16. (currently amended) A method of operating ~~an N_logalu~~ a first number of a logalu using a wide instruction, comprising the steps of:

~~providing a narrow instruction to~~ a local wide instruction memory receiving a narrow instruction;

said local wide instruction memory responding to said narrow instruction to at least partly create said wide instruction;

said logalu receiving said wide instruction;

~~configuring~~ said logalu configured based upon said wide instruction to operate upon ~~N_log_operands~~ a second number of a log-operand;

wherein said ~~N_logalu~~ first number is at least one; and

wherein said ~~N_log_operands~~ second number is at least two.

17. (Original) The method of Claim 16, wherein said ~~N_logalu~~ first number is at least two.

18. (Original) The method of Claim 17, wherein the step of said logalu receiving said wide instruction is further comprised, for each of said logalus, of the step of:

said logalu receiving said wide instruction.

19. (Original) The method of Claim 17, wherein said wide instruction for at least two of said logalus is at least partly distinct.

20. (cancelled) The method of Claim 18, wherein the step said local wide instruction memory responding to said narrow instruction is further comprised of the step of:

said local wide instruction memory responding to said narrow instruction to at least partly create said wide instruction associated with said logalu, for each of said logalus;

~~wherein said wide instructions associated with at least two of said logalus are at least partly distinct~~.

21. (currently amended) The method of Claim 16, wherein said narrow instruction is comprised of a designator field, a first narrow field and a second narrow field;

wherein the step said local wide instruction memory responding to said narrow instruction, is further comprised of the steps of:

a selection configuration circuit selecting from said first narrow field and said second narrow field based upon said designator field to provide a selected narrow instruction to ~~a~~ said local wide memory; and

said local wide memory responding to said selected narrow instruction to at least partly create said wide instruction.

22. (currently amended) The method of Claim 21, wherein the step of selecting is further comprised of the steps of:

~~presenting said designator field to a~~ said selection configuration circuit presented said designator field; and

~~said selection configuration circuit~~ selecting from said first narrow field and said second narrow field based upon a response from said selection configuration circuit to said designator field.

23. (currently amended) The method of Claim 22, further comprising the steps of:

~~providing a configuration signal to~~ said selection configuration circuit provided said configuration signal; and

~~altering a state in~~ said selection configuration circuit altering its state based upon said configuration signal.

24. (Original) The method of Claim 23, wherein said state resides in a selection configuration memory included in said selection configuration circuit.

25. (currently amended) The method of Claim 16, further comprising the step of:

~~providing~~ said local wide instruction memory provided with a write instruction;

wherein the step of said local wide instruction memory responding to said narrow instruction is at least partly altered based upon said write instruction.

26. (currently amended) A method of generating a non-additive result based upon said N_log_operands of a log-operand of Claim 16, comprising the steps of:

~~operating~~ a logalu operated by the steps of Claim 16,

~~providing said log-operands to~~ said logalu provided said log operands;

said logalu responding to said log-operands and to said wide instruction to create a log-result presented to a exponential calculator; and

said exponential calculator responding to said log-result to create said non-additive result.

27. (Original) The method of Claim 26, wherein said non-additive result includes a first multiplicative component and a second multiplicative component;

wherein said first multiplicative component is a member of the non-

additive primitive collection based upon a first of said log-operands;

wherein said second multiplicative component is a member of said non-additive primitive collection based upon a second of said log-operands;

wherein said non-additive primitive collection based upon one of said log-operands includes:

an exponential of said one log-operand,

an exponential of a half of said one log-operand,

an exponential of a negative of said one log-operand,

an exponential of a negative of said half of said one log-operand,

an exponential of a double of said one log-operand, and

an exponential of a negative of said double of said one log-operand.

28. (Original) The method of Claim 27, further comprising the step of:

a log-calculator providing said first log-operand based upon a first operand;

wherein said non-additive primitive collection based upon one of said log-operands includes:

an approximation of said first operand,

an approximation of a square root of said first operand,

an approximation of a multiplicative inverse of said first operand,

an approximation of a multiplicative inverse of said square root of said first operand,

an approximation of a square of said first operand, and

an approximation of a multiplicative inverse of said square of said first operand.

29. (Original) The method of Claim 28, wherein said approximations satisfy a precision standard.

30. (Original) The method of Claim 29, wherein said precision standard supports a member of the programming languages collection comprising: a version of

Java, a version of C, a version of OpenGL, and a version of DirectX.

Consequently the Examiner is requested the removal of this rejection from these Claims.

Request for telephone interview if this application is not in condition for allowance

The Applicant believes that this application is in condition for allowance and requests that if the Examiner does not find this application in condition for allowance, that Earle Jennings be contacted for a telephone interview to discuss how to expedite the application's prosecution.

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